WHAT IS CLAIMED IS:

1. A shift register, comprising:

flip flops of a plurality of steps that operate in synchronization with a clock signal, and

a level shifter for increasing a voltage of a clock signal smaller in an amplitude than a driving voltage of said flip flop and for applying the clock signal to each of said flip flops, said shift register transmitting an input pulse in synchronization with the clock signal,

wherein said flip flops are divided into a plurality of blocks, each including at least one of said flip flops,

said level shifter is provided for each of said blocks, and

among a plurality of said level shifters, at least one of said level shifters, which correspond to blocks requiring no clock signal input for transmitting the input pulse, is suspended at that point.

2. The shift register as defined in claim 1, wherein at least one of said level shifters operates only when a corresponding block includes said flip flop requiring a clock signal input at that point.

3. The shift register as defined in claim 1, wherein each of said level shifters operates only when a

corresponding block includes said flip flop requiring a clock signal input at that point.

4. The shift register as defined in claim 1, wherein a specific block of said blocks includes a set reset flip flop serving as said flip flop, said set reset flip flop being set in response to the clock signal, and

a specific level shifter corresponding to the specific block starts an operation at a start of a pulse input to the specific block and is suspended after setting said flip flop of a final step in the specific block.

5. The shift register as defined in claim 4, wherein said specific block includes one of said flip flops, and

said specific level shifter starts an operation at a start of a pulse input to the specific block and is suspended at an end of the pulse input.

6. The shift register as defined in claim 4, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter operates during a pulse input to said specific block and during a pulse output of any one of said flip flops in a step except for the final step in the specific block.

7. The shift register as defined in claim 4, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter includes a latch circuit which changes an output in response to a signal inputted to said specific block and an output signal of said flip flop in the final step of said specific block.

8. The shift register as defined in claim 1, wherein a specific block of said blocks includes a D flip flop as said flip flop, and

a specific level shifter corresponding to the specific block starts an operation at a start of a pulse input to the specific block and is suspended after a pulse output of said flip flop of a final step in the specific block.

9. The shift register as defined in claim 8, wherein said specific block includes a plurality of said flip flops, and

said specific level shifter includes a latch circuit which changes an output in response to a signal inputted to said specific block and an output signal of said flip flop in the final step of said specific block.

10. The shift register as defined in claim 1, wherein

said level shifter includes a current-driven level shift section provided with an input switching element.

11. The shift register as defined in claim 10, wherein said level shifter includes an input signal control section which suspends said level shifter by providing a signal at a level for interrupting said input switching element.

12. The shift register as defined in claim 10, wherein said level shifter includes a power supply control section for suspending power supply to said level shift section so as to suspend said level shifter.

13. The shift register as defined in claim 1, wherein each of said level shifters includes output stabilizing means.

14. The shift register as defined in claim 13, wherein said level shifter includes a clock signal line for transmitting the clock signal, and a switch which is disposed between said clock signal line and said level shift section and is opened during suspension of said level shifter.

15. An image display apparatus comprising data signal

extracting means for extracting a data signal corresponding to each pixel from an image signal in synchronization with a clock signal, and data signal output means for outputting the data signal to each of the pixels,

wherein said data signal extracting means includes said shift register defined in claim 1.

16. An image display apparatus comprising:

a plurality of pixels disposed in a matrix form,

a plurality of data signal lines disposed for each row of said pixels,

a plurality of scanning lines disposed for each column of said pixels,

a scanning signal line driving circuit for successively applying a scanning signal with different timings to each of said scanning signal lines in synchronization with a first clock signal having a predetermined period, and

a data signal line driving circuit for extracting a data signal from an image signal applied to each of said pixels on said scanning line where the scanning signal is applied, and for outputting the data signal to said data signal lines, said image signal being successively applied in synchronization with a second clock signal having a predetermined period, said image signal indicating a display state of each of said pixels,

wherein at least one of said data signal line driving circuit and said scanning signal line driving circuit is provided with said shift register defined in claim 1, in which the first or second clock signal serves as said clock signal.

17. The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels are formed on the same substrate.

18. The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels include a switching element composed of a polycrystalline silicon thin film transistor.

19. The image display apparatus as defined in claim 16, wherein said data signal line driving circuit, said scanning signal line driving circuit, and said pixels include a switching element manufactured at a process temperature of 600°C or less.

20. A shift register, in which a plurality of flip flops connected, comprising a plurality of level shifters

for level-shifting a clock signal, said level shifter being provided for every predetermined number of said flip flops.

21. The shift resister as defined in claim 20, wherein at least one of a plurality of said level shifters is suspended.